

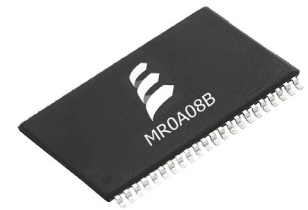
FEATURES

- 3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Native non-volatility
- Unlimited read & write endurance
- Data always non-volatile for >20 years at temperature
- Commercial and industrial temperatures
- All products meet MSL-3 moisture sensitivity level
- RoHS-Compliant TSOP2 and BGA packages

128K x 8 MRAM



48-ball FBGA



44-pin TSOP2

BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and MRAM in system for simpler, more efficient design
- Improves reliability by replacing battery-backed SRAM

INTRODUCTION

The **MR0A08B** is a 1,048,576-bit magnetoresistive random access memory (MRAM) device organized as 131,072 words of 8 bits. The MR0A08B offers SRAM compatible 35 ns read/write timing with unlimited endurance.

Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR0A08B is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The **MR0A08B** is available in small footprint 400-mil, 44-lead plastic small-outline TSOP type-2 package, 8 mm x 8 mm, or a 48-pin ball grid array (BGA) package with 0.75 mm ball centers. (The 32-SOIC package options is obsolete and no longer available for new orders.) These packages are compatible with similar low-power SRAM products and other non-volatile RAM products.

The **MR0A08B** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature range (0 to +70 °C) and industrial temperature range (-40 to +85 °C).



TABLE OF CONTENTS

FEATURES	1
BENEFITS.....	1
INTRODUCTION	1
BLOCK DIAGRAM AND PIN ASSIGNMENTS	4
Figure 1 – MR0A08B Block Diagram	4
Table 1 – Pin Functions	4
Figure 2 – Pin Diagrams for Available Packages (Top View) ¹	5
OPERATING MODES	5
Table 2 – Operating Modes	5
ELECTRICAL SPECIFICATIONS	6
Table 3 – Absolute Maximum Ratings.....	6
OPERATING CONDITIONS	7
Table 4 – Operating Conditions.....	7
Power Up and Power Down Sequencing	8
Figure 3 – Power Up and Power Down Diagram.....	8
DC CHARACTERISTICS	9
Table 5 – DC Characteristics.....	9
Table 6 – Power Supply Characteristics	9
TIMING SPECIFICATIONS	10
Table 7 – Capacitance	10
Table 8 – AC Measurement Conditions	10
Figure 4 – Output Load Test Low and High.....	10
Figure 5 – Output Load Test All Others.....	10

TABLE OF CONTENTS (CONT'D)

Read Mode	11
Table 9 – Read Cycle Timing	11
Figure 6 – Read Cycle 1	12
Figure 7 – Read Cycle 2	12
Write Mode	13
Table 10 – Write Cycle Timing 1 ($\overline{W}$ Controlled)	13
Figure 8 – Write Cycle Timing 1 ($\overline{W}$ Controlled)	14
Table 11 – Write Cycle Timing 2 ($\overline{E}$ Controlled)	15
Figure 9 – Write Cycle Timing 2 ($\overline{E}$ Controlled)	16
Table 12 – Write Cycle Timing 3 (Shortened t_{WHAX} , $\overline{W}$ and $\overline{E}$ Controlled)	17
Figure 10 – Write Cycle Timing 3 (Shortened t_{WHAX} , $\overline{W}$ and $\overline{E}$ Controlled)	17
ORDERING INFORMATION	18
Table 13 – Ordering Part Number System for Parallel I/O MRAM	18
Table 14 – MR0A08B Ordering Part Numbers ¹	18
PACKAGE OUTLINE DRAWINGS	19
Figure 11 – 44-TSOP2 Package Outline	19
Figure 12 – 48-BGA Package Outline	20
Figure 13 – 32-SOIC Package Outline ¹	21
REVISION HISTORY	22
HOW TO CONTACT US	23

BLOCK DIAGRAM AND PIN ASSIGNMENTS

Figure 1 – MR0A08B Block Diagram

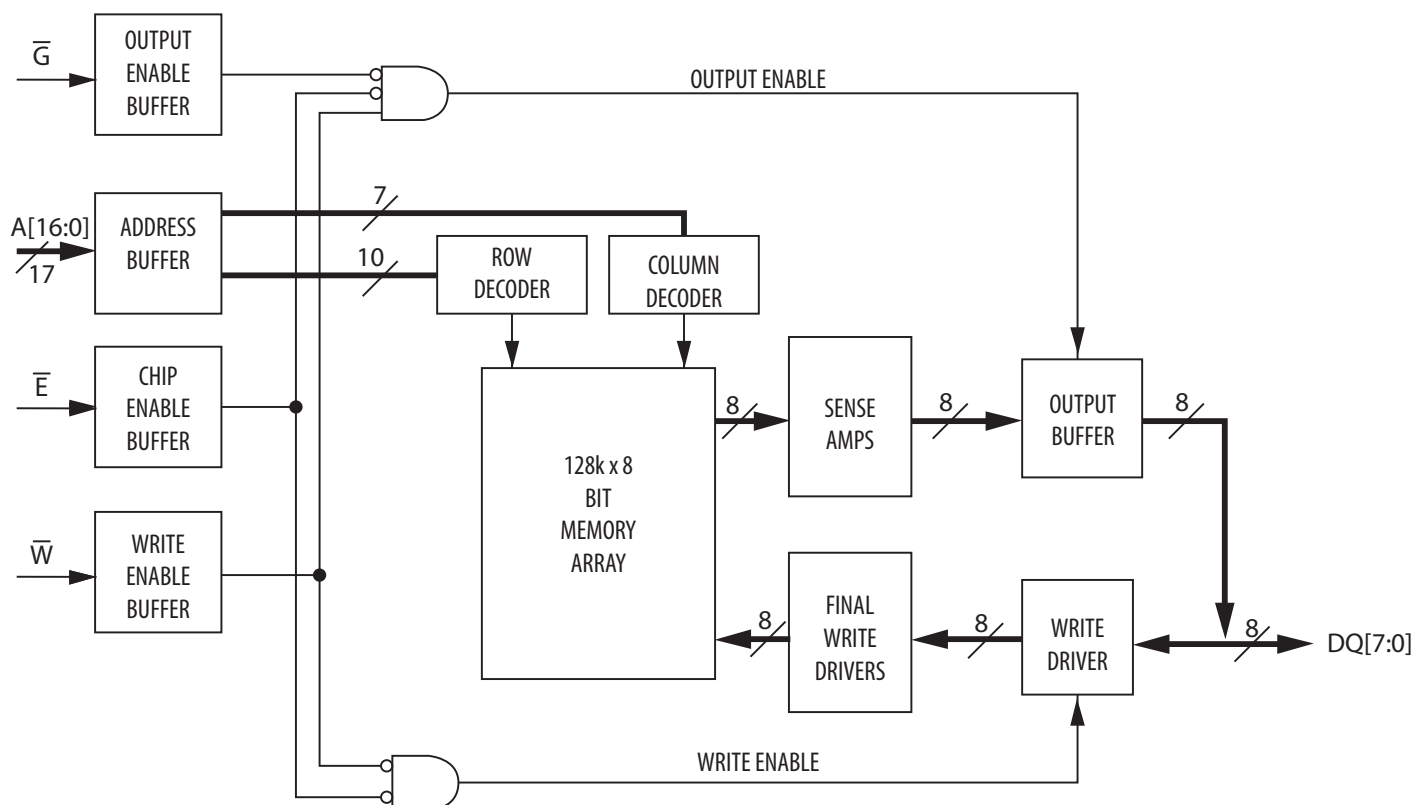
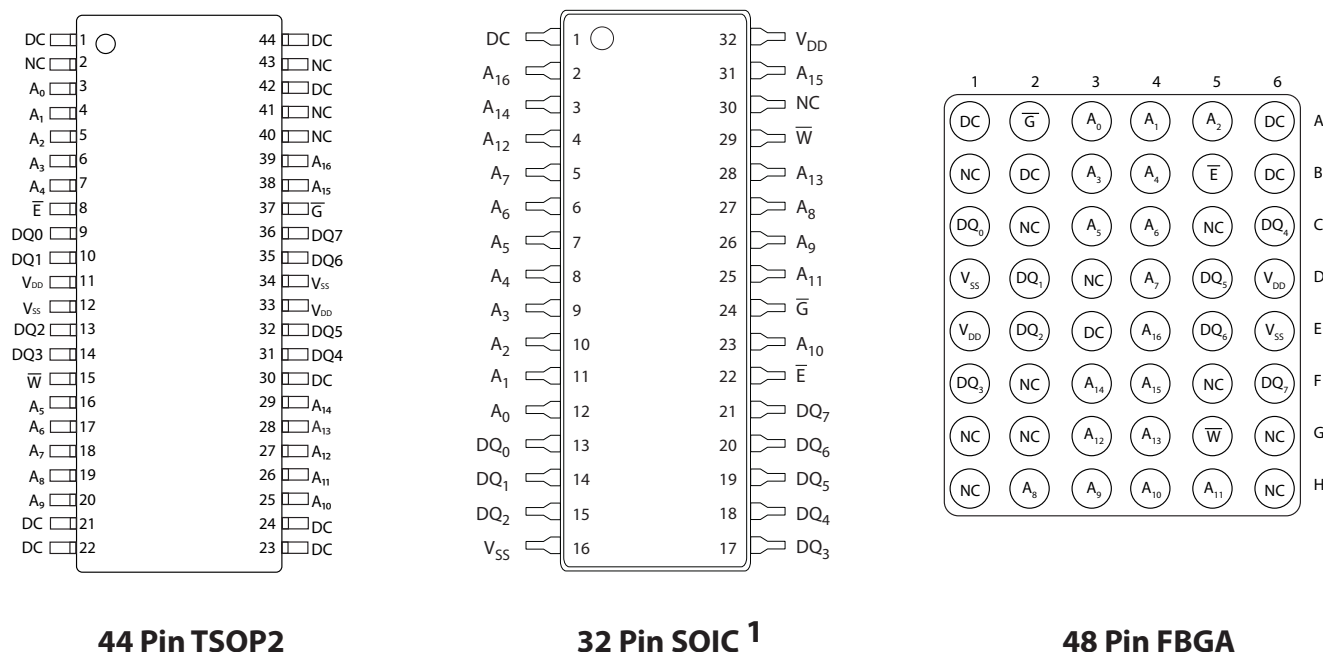


Table 1 – Pin Functions

Signal Name	Function
A	Address Input
$\bar{E}$	Chip Enable
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection - Pin 2, 40, 41, 43 (TSOP2); Ball C2, C5, D3, F2, F5, G1, G2, G6, H1, H6 (BGA); Pin 30 (SOIC) Reserved For Future Expansion

Figure 2 – Pin Diagrams for Available Packages (Top View) ¹



Note:

1. The 32-SOIC package is obsolete and shown for legacy reference only. This package option is no longer available for new orders.

OPERATING MODES

Table 2 – Operating Modes

$\bar{E}$ ¹	$\bar{G}$ ¹	$\bar{W}$ ¹	Mode	V _{DD} Current	DQ[7:0] ²
H	X	X	Not selected	I _{SB1} , I _{SB2}	Hi-Z
L	H	H	Output disabled	I _{DDR}	Hi-Z
L	L	H	Byte Read	I _{DDR}	D _{Out}
L	X	L	Byte Write	I _{DDW}	D _{in}

Notes:

1. H = high, L = low, X = don't care
2. Hi-Z = high impedance

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings. ¹

Table 3 – Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ^{2,3}	V_{DD}	-0.5 to 4.0	V
Voltage on any pin ^{2,3}	V_{IN}	-0.5 to $V_{DD} + 0.5$	V
Output current per pin	I_{OUT}	±20	mA
Package power dissipation ³	P_D	0.600	W
Temperature under bias MR0A08B (Commercial) MR0A08BC (Industrial)	T_{BIAS}	-10 to 85 -45 to 95	°C
Storage Temperature	T_{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write MR0A08B (All Temperatures)	H_{max_write}	2000	A/m
Maximum magnetic field during read or standby	H_{max_read}	8000	A/m

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS} .
3. Power dissipation capability depends on package characteristics and use environment.

OPERATING CONDITIONS

Table 4 – Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	V_{DD}	3.0 ¹	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0 ¹	V
Input high voltage	V_{IH}	2.2	-	$V_{DD} + 0.3$ ²	V
Input low voltage	V_{IL}	-0.5 ³	-	0.8	V
Temperature under bias					
MR0A08B (Commercial)	T_A	0		70	°C
MR0A08BC (Industrial)		-40		85	

Notes:

1. There is a 2 ms startup time once V_{DD} exceeds $V_{DD, (max)}$. See “Figure 3 – Power Up and Power Down Diagram”.
2. $V_{IH(max)} = V_{DD} + 0.3 V_{DC}$; $V_{IH(max)} = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
3. $V_{IL(min)} = -0.5 V_{DC}$; $V_{IL(min)} = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

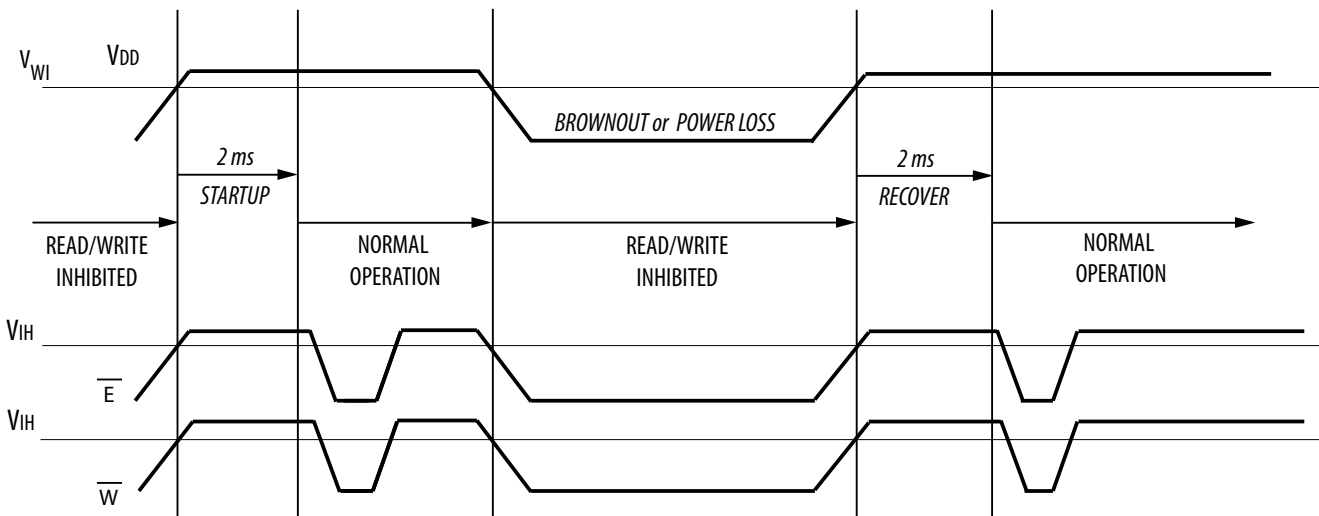
Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD}(\min)$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\bar{E}$ and $\bar{W}$ control signals should track V_{DD} on power up to $V_{DD} - 0.2\text{ V}$ or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives $\bar{E}$ and $\bar{W}$ should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD}(\min)$.

Figure 3 – Power Up and Power Down Diagram



DC CHARACTERISTICS

Table 5 – DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	$I_{lkg(I)}$	-	-	± 1	μA
Output leakage current	$I_{lkg(O)}$	-	-	± 1	μA
Output low voltage ($I_{OL} = +4 \text{ mA}$) ($I_{OL} = +100 \mu A$)	V_{OL}	-	-	0.4 $V_{SS} + 0.2$	V
Output high voltage ($I_{OL} = -4 \text{ mA}$) ($I_{OL} = -100 \mu A$)	V_{OH}	2.4 $V_{DD} - 0.2$	-	-	V

Table 6 – Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
AC active supply current - read modes ¹ ($I_{OUT} = 0 \text{ mA}$, $V_{DD} = \text{max}$)	I_{DDR}	25	30	mA
AC active supply current - write modes ¹ ($V_{DD} = \text{max}$) MR0A08B (Commercial) MR0A08BC (Industrial)	I_{DDW}	55 55	65 70	mA
AC standby current ($V_{DD} = \text{max}$, $\bar{E} = V_{IH}$) <i>no other restrictions on other inputs</i>	I_{SB1}	6	7	mA
CMOS standby current ($\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}$, $f = 0 \text{ MHz}$)	I_{SB2}	5	6	mA

Notes:

1. All active current measurements are measured with one address transition per cycle and at minimum cycle time.

TIMING SPECIFICATIONS

Table 7 – Capacitance

Parameter ¹	Symbol	Typical	Max	Unit
Address input capacitance	C_{In}	-	6	pF
Control input capacitance	C_{In}	-	6	pF
Input/Output capacitance	$C_{I/O}$	-	8	pF

Notes:

1. $f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25^\circ \text{C}$, periodically sampled rather than 100% tested.

Table 8 – AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 4	
Output load for all other timing parameters	See Figure 5	

Figure 4 – Output Load Test Low and High

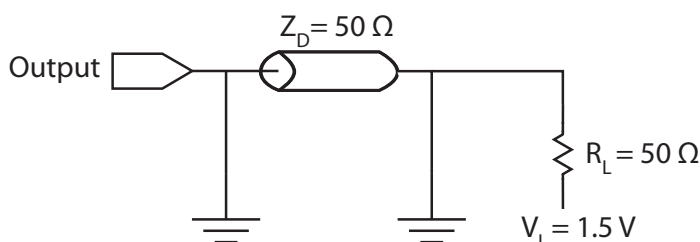
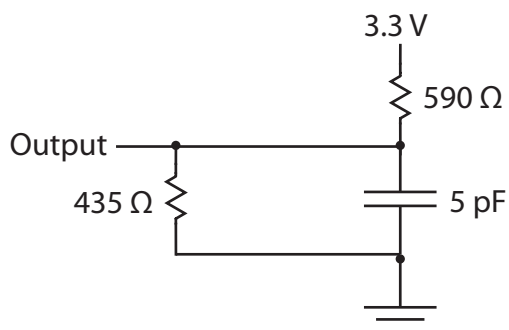


Figure 5 – Output Load Test All Others



Read Mode

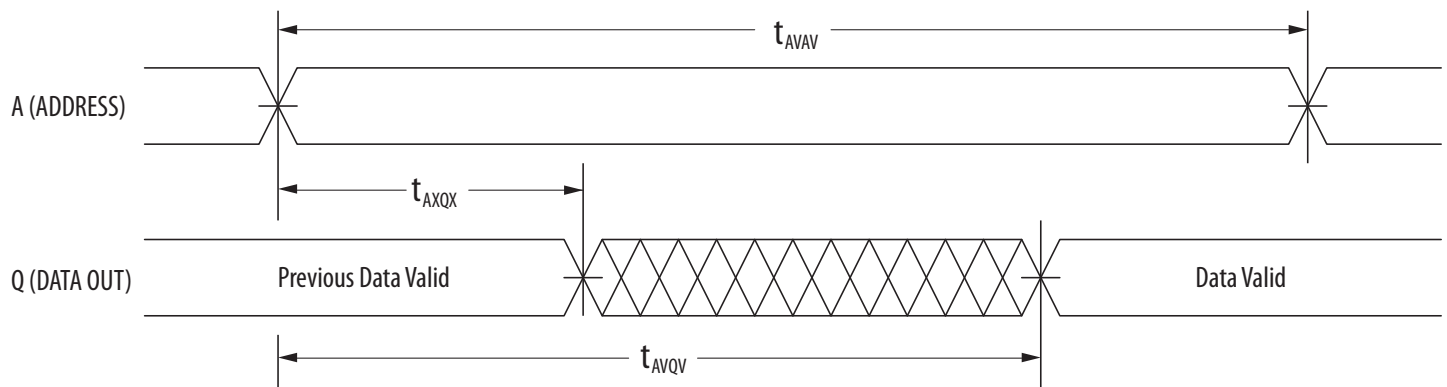
Table 9 – Read Cycle Timing

Parameter ¹	Symbol	Min	Max	Unit
Read cycle time	t _{AVAV}	35	-	ns
Address access time	t _{AVQV}	-	35	ns
Enable access time ²	t _{ELQV}	-	35	ns
Output enable access time	t _{GLQV}	-	15	ns
Output hold from address change	t _{AXQX}	3	-	ns
Enable low to output active ³	t _{ELQX}	3	-	ns
Output enable low to output active ³	t _{GLQX}	0	-	ns
Enable high to output Hi-Z ³	t _{EHQZ}	0	15	ns
Output enable high to output Hi-Z ³	t _{GHQZ}	0	10	ns

Notes:

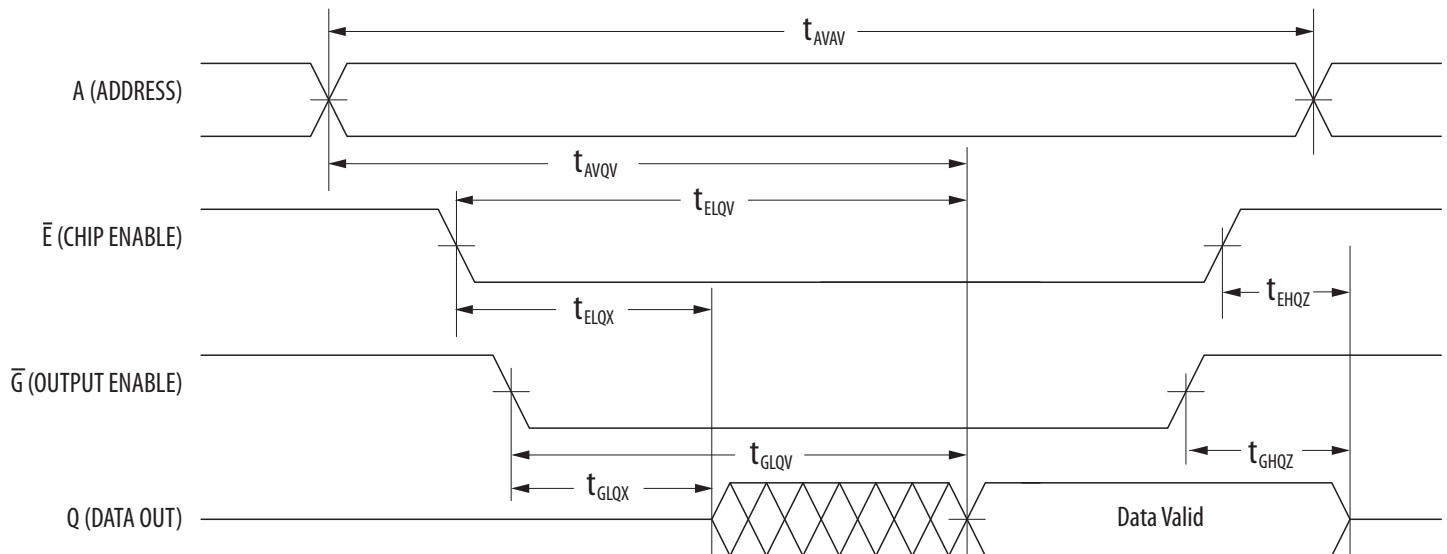
1. $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2. Addresses valid before or at the same time $\overline{E}$ goes low.
3. This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage.

Figure 6 – Read Cycle 1



Note: Device is continuously selected ($\bar{E} \leq V_{IL}$, $\bar{G} \leq V_{IL}$).

Figure 7 – Read Cycle 2



Write Mode

Table 10 – Write Cycle Timing 1 ($\overline{W}$ Controlled)

Parameter ¹	Symbol	Min	Max	Unit
Write cycle time ²	t_{AVAV}	35	-	ns
Address set-up time	t_{AVWL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	18	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVWH}	20	-	ns
Write pulse width ($\overline{G}$ high)	t_{WLWH} t_{WLEH}	15	-	ns
Write pulse width ($\overline{G}$ low)	t_{WLWH} t_{WLEH}	15	-	ns
Data valid to end of write	t_{DVWH}	10	-	ns
Data hold time	t_{WHDX}	0	-	ns
Write low to data Hi-Z ³	t_{WLQZ}	0	12	ns
Write high to output active ³	t_{WHQX}	3	-	ns
Write recovery time	t_{WHAX}	12	-	ns

Notes:

1. All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$ or $\overline{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperature, $t_{WLQZ}(\text{max}) < t_{WHQX}(\text{min})$

Figure 8 – Write Cycle Timing 1 ($\overline{W}$ Controlled)

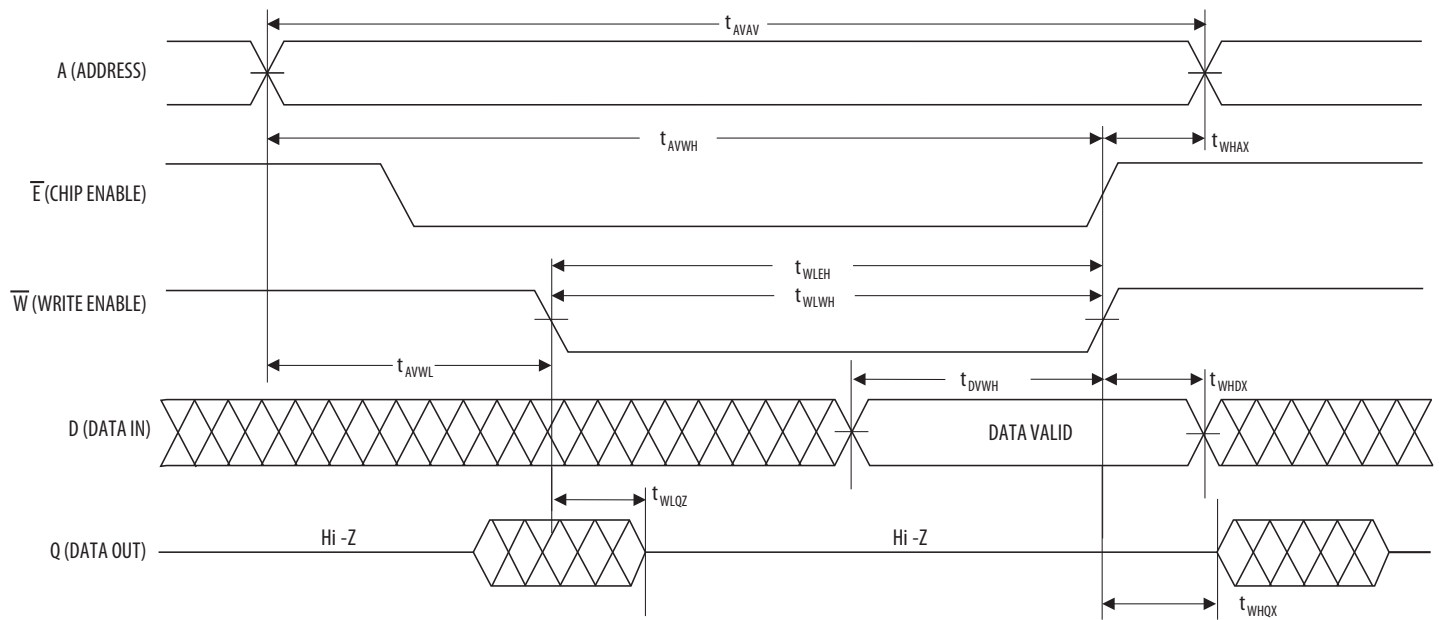


Table 11 – Write Cycle Timing 2 ($\bar{E}$ Controlled)

Parameter ¹	Symbol	Min	Max	Unit
Write cycle time ²	t_{AVAV}	35	-	ns
Address set-up time	t_{AVEL}	0	-	ns
Address valid to end of write ($\bar{G}$ high)	t_{AVEH}	18	-	ns
Address valid to end of write ($\bar{G}$ low)	t_{AVEH}	20	-	ns
Enable to end of write ($\bar{G}$ high)	t_{ELEH} t_{ELWH}	15	-	ns
Enable to end of write ($\bar{G}$ low) ³	t_{ELEH} t_{ELWH}	15	-	ns
Data valid to end of write	t_{DVEH}	10	-	ns
Data hold time	t_{EHDX}	0	-	ns
Write recovery time	t_{EHAX}	12	-	ns

Notes:

1. All write occurs during the overlap of $\bar{E}$ low and $\bar{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\bar{G}$ goes low at the same time or after $\bar{W}$ goes low, the output will remain in a high impedance state. After $\bar{W}$ or $\bar{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\bar{E}$ being asserted low in one cycle to $\bar{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If $\bar{E}$ goes low at the same time or after $\bar{W}$ goes low, the output will remain in a high-impedance state. If $\bar{E}$ goes high at the same time or before $\bar{W}$ goes high, the output will remain in a high-impedance state.

Figure 9 – Write Cycle Timing 2 ($\bar{E}$ Controlled)

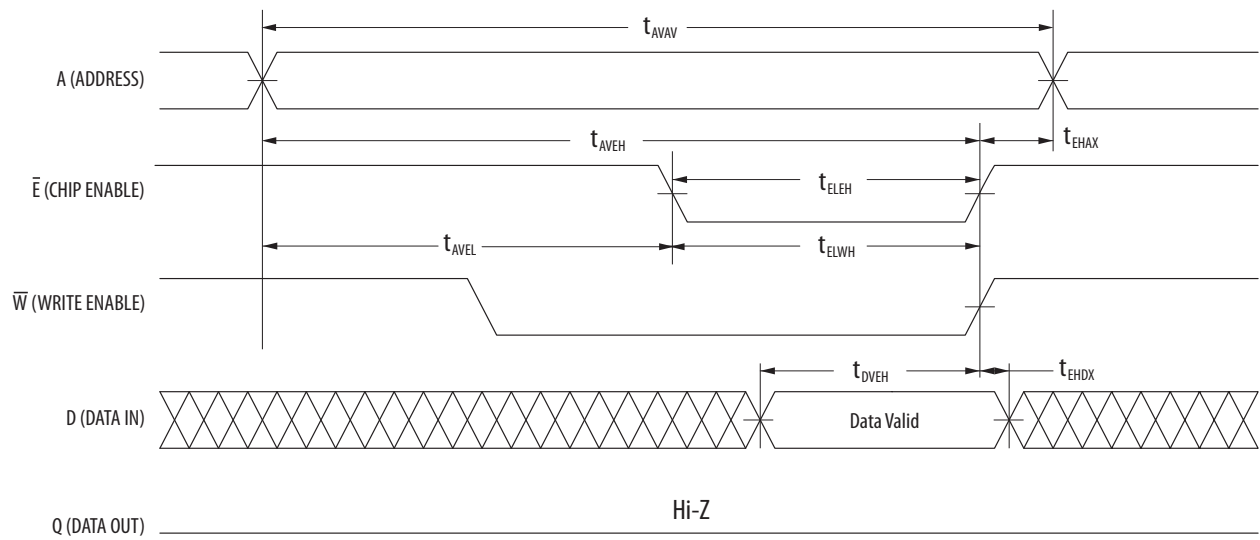


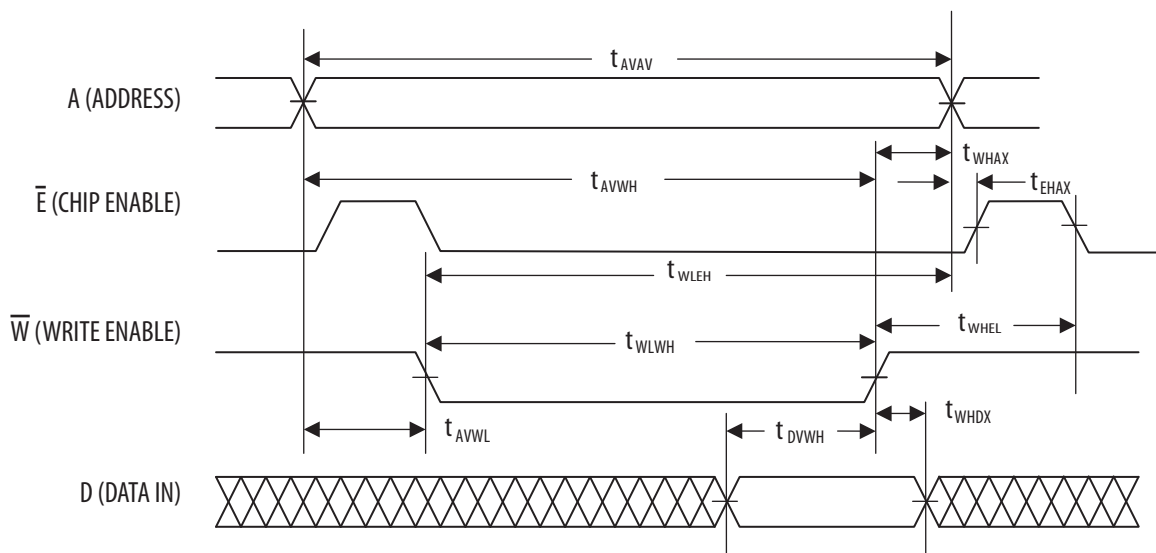
Table 12 – Write Cycle Timing 3 (Shortened t_{WHAX} , $\overline{W}$ and $\overline{E}$ Controlled)

Parameter ¹	Symbol	Min	Max	Unit
Write cycle time ²	t_{AVAV}	35	-	ns
Address set-up time	t_{AVWL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	18	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVWH}	20	-	ns
Write pulse width	t_{WLWH} t_{WLEH}	15	-	ns
Data valid to end of write	t_{DVWH}	10	-	ns
Data hold time	t_{WHDX}	0	-	ns
Enable recovery time	t_{EHAX}	-2	-	ns
Write recovery time ³	t_{WHAX}	6	-	ns
Write to enable recovery time ³	t_{WHEL}	12	-	ns

Notes:

1. All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, or $\overline{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low the output will remain in a high impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high the output will remain in a high impedance state. $\overline{E}$ must be brought high each cycle.

Figure 10 – Write Cycle Timing 3 (Shortened t_{WHAX} , $\overline{W}$ and $\overline{E}$ Controlled)



ORDERING INFORMATION

Table 13 – Ordering Part Number System for Parallel I/O MRAM

Example Ordering Part Number		Memory	Density	Type	I/O Width	Rev.	Temp	Package	Speed	Packing	Grade
MRAM	MR	MR	0	A	08	B	C	MA	35	R	
256 Kb	256										
1 Mb	0										
4 Mb	2										
16 Mb	4										
Async 3.3v	A										
Async 3.3v Vdd and 1.8v Vddq	D										
Async 3.3v Vdd and 1.8v Vddq with 2.7v min. Vdd	DL										
8-bit	08										
16-bit	16										
Rev A	A										
Rev B	B										
Commercial	0 to 70°C	Blank									
Industrial	-40 to 85°C	C									
Extended	-40 to 105°C	V									
AEC Q-100 Grade 1	-40 to 125°C	M									
44-TSOP-2	YS										
48-FBGA	MA										
16-SOIC	SC										
32-SOIC	SO										
35 ns	35										
45 ns	45										
Tray	Blank										
Tape and Reel	R										
Engineering Samples	ES										
Customer Samples	Blank										
Mass Production	Blank										

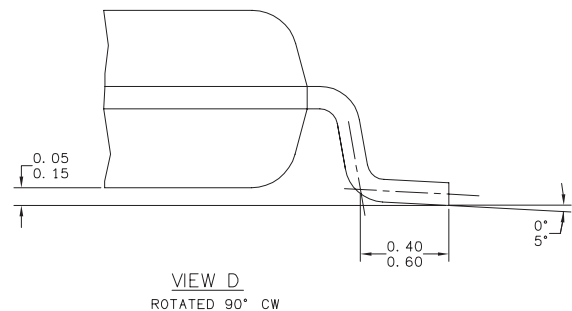
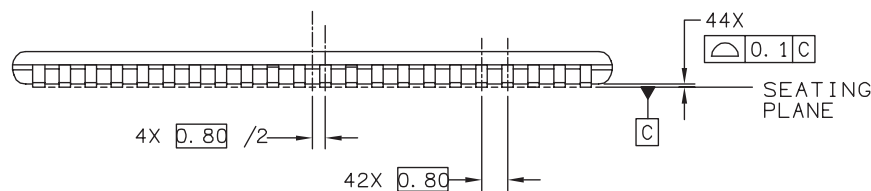
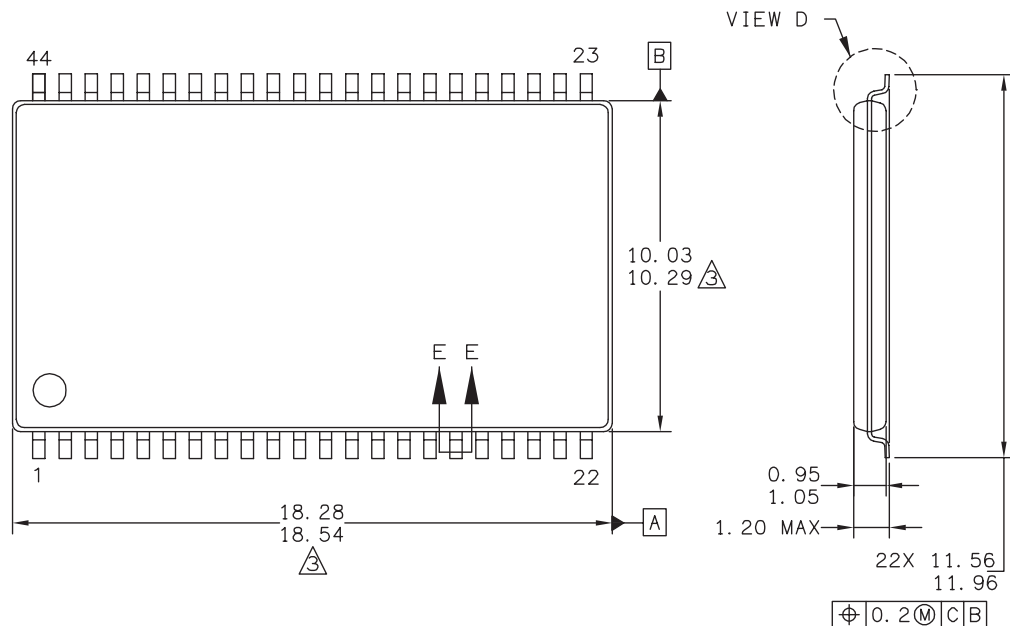
Table 14 – MR0A08B Ordering Part Numbers ¹

Temp Grade	Temp	Package	Shipping	Ordering Part Number
Commercial	0 to +70 °C	44-TSOP2	Tray	MR0A08BYS35
			Tape and Reel	MR0A08BYS35R
		48-BGA	Tray	MR0A08BMA35
			Tape and Reel	MR0A08BMA35R
		32-SOIC ¹	Tray	MR0A08BSO35 Obsolete
			Tape and Reel	MR0A08BSO35R Obsolete
Industrial	-40 to +85 °C	44-TSOP2	Tray	MR0A08BCYS35
			Tape and Reel	MR0A08BCYS35R
		48-BGA	Tray	MR0A08BCMA35
			Tape and Reel	MR0A08BCMA35R
		32-SOIC ¹	Tray	MR0A08BCSO35 Obsolete
			Tape and Reel	MR0A08BCSO35R Obsolete

¹ The 32-SOIC package option is obsolete and no longer available. See PCN02895 [here](#).

PACKAGE OUTLINE DRAWINGS

Figure 11 – 44-TSOP2 Package Outline



Not To Scale

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.
5. DAM Bar protrusion shall not cause the lead width to exceed 0.58.

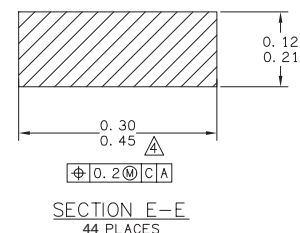
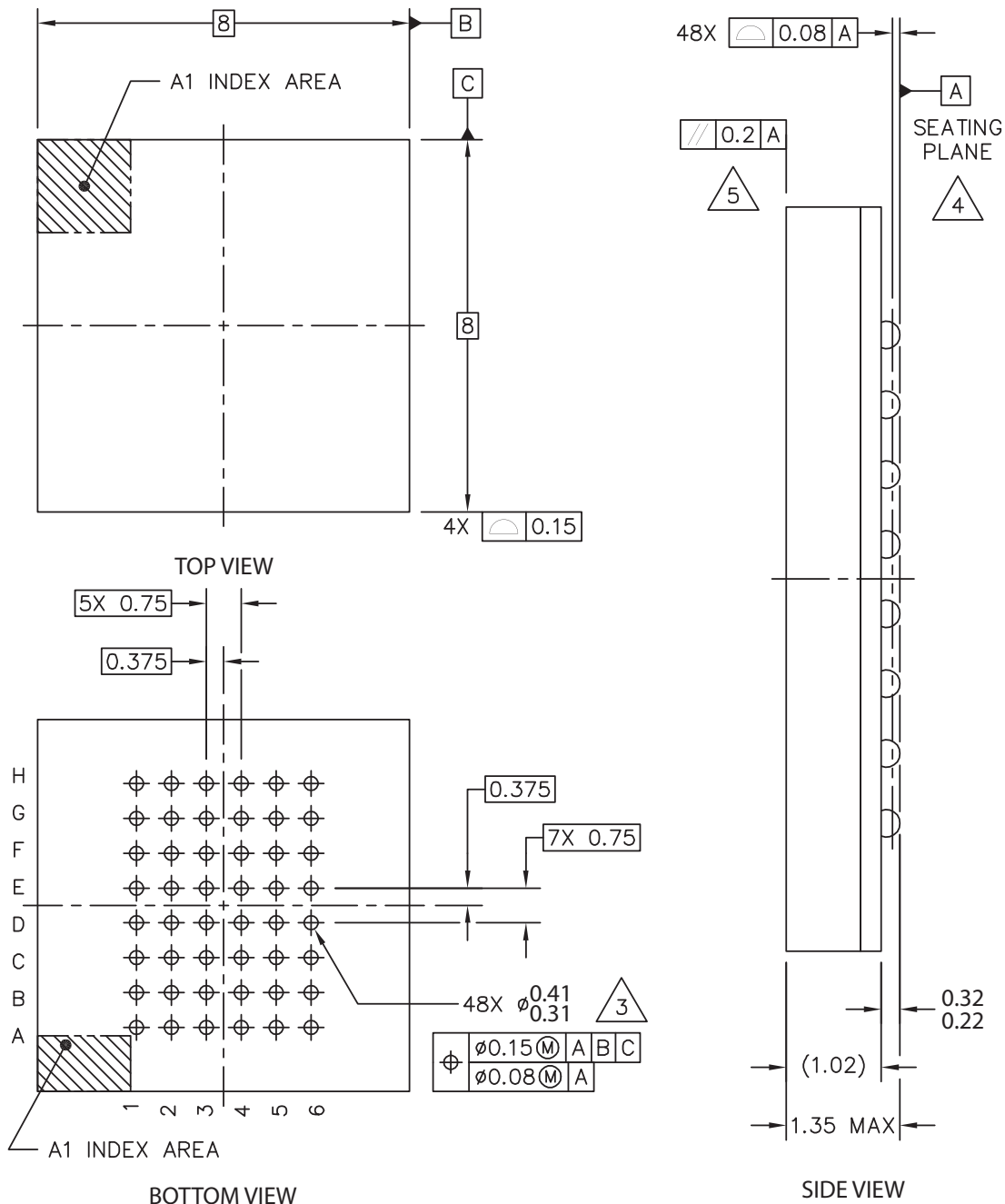


Figure 12 – 48-BGA Package Outline



Not To Scale

1. Dimensions in Millimeters.

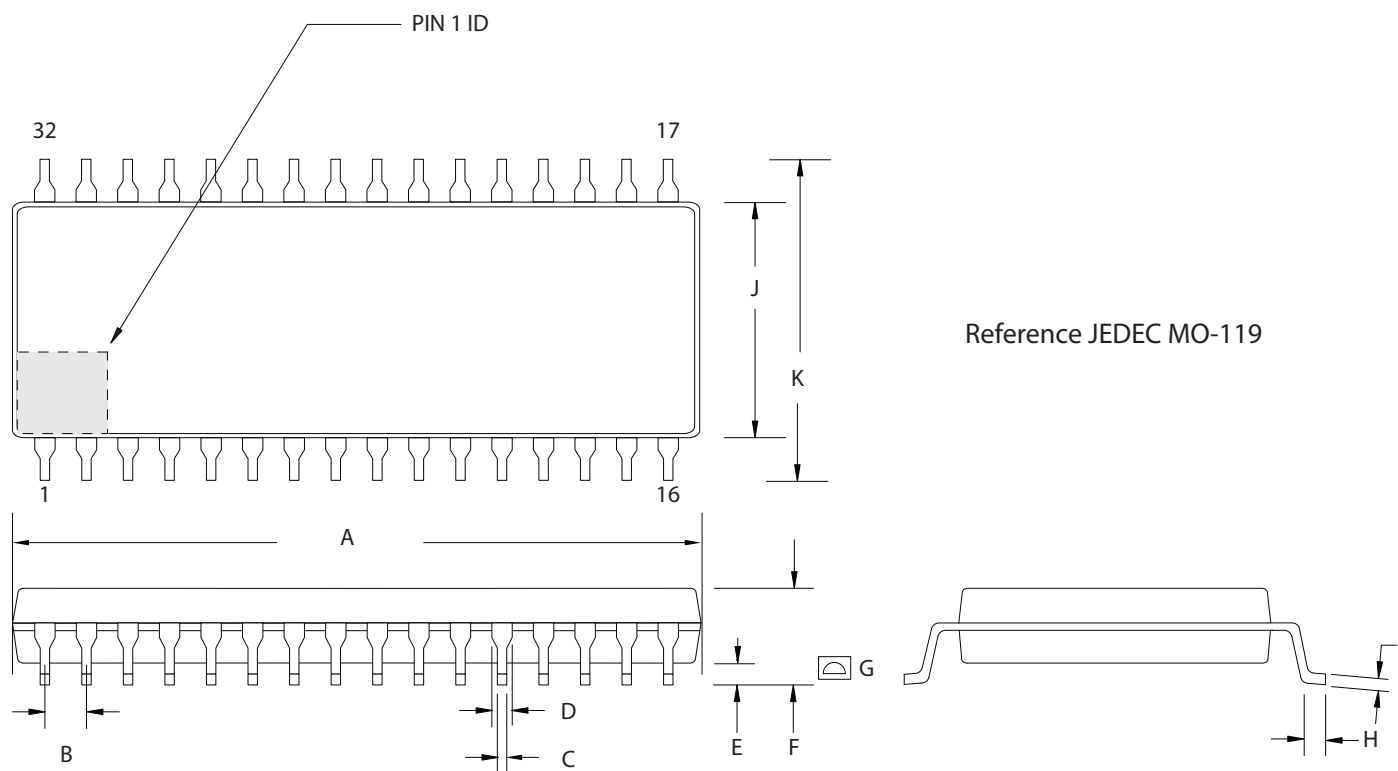
2. Dimensions and tolerances per ASME Y14.5M - 1994.

3. Maximum solder ball diameter measured parallel to DATUM A

4. DATUM A, the seating plane is determined by the spherical crowns of the solder balls.

5. Parallelism measurement shall exclude any effect of mark on top surface of package.

Figure 13 – 32-SOIC Package Outline ¹



Unit	A	B	C	D	E	F	G	H	I	J	K
mm - Min	20.574	1.00	0.355	0.66	0.101	2.286	Radius	0.533	0.152	7.416	10.287
- Max	20.878	1.50	0.508	0.81	0.254	2.540	0.101	1.041	0.304	7.594	10.642
inch - Min	0.810	0.04	0.14	0.026	0.004	0.09	Radius	0.021	0.006	0.292	0.405
- Max	0.822	0.06	0.02	0.032	0.010	0.10	0.0040	0.041	0.012	0.299	0.419

Note:

1. The 32-SOIC package is obsolete and shown for legacy reference only. This package option is no longer available for new orders.

REVISION HISTORY

Revision	Date	Description of Change
0	Sep 12, 2008	Initial Advance Information Release
1	May 8, 2009	Revised format; Add Table 3.6 Write Timing Cycle 3; Add Figure 3.6 Write Timing Cycle 3; Add TSOPII Lead Width Info; Changed to Preliminary from Product Concept.
2	June 18, 2009	Changed from datasheet from Preliminary to Production except where noted.
3	Apr 12, 2011	Added SOIC package option.
4	August 15, 2011	Corrected SOIC Pin 1 to read DC. Updated contact information. Revised copyright year.
5	Dec 16, 2011	Changed TSOP-II to TSOP2. Changed logo to new EST Logo. Added Industrial Temp Grade option in SOIC package, Table 4.1. Deleted Tape & Reel pack option for all SOIC packaged parts. Figure 2.1 cosmetic update. Figure 5.2 BGA package outline drawing revised for ball size.
6	July 9, 2013	MR0A08BCSO35 preliminary status removed. Now MP.
7	September 4, 2013	Added table of dimensions to the SOIC package outline diagram.
8	October 11, 2013	Added Tape and Reel shipping option for SOIC packaged versions. Reformatted to current standards.
8.1	May 18, 2015	Revised How to Contact Us information.
8.2	June 11, 2015	Correction to Japan Sales Office telephone number.
8.3	July 20, 2015	32-SOIC package options Not Recommended for New Designs.
8.4	October 17, 2015	32-SOIC package options are obsolete and no longer available.
8.5	December 9, 2015	Corrections to incorrect package pinouts and replaced missing 48-BGA package outline drawing.
8.6	March 22, 2018	Updated Contact Us table

HOW TO CONTACT US

Home Page:

www.everspin.com

World Wide Information Request

WW Headquarters - Chandler, AZ

5670 W. Chandler Blvd., Suite 100

Chandler, Arizona 85224

Tel: +1-877-480-MRAM (6726)

Local Tel: +1-480-347-1111

Fax: +1-480-347-1175

support@everspin.com

Europe, Middle East and Africa

Everspin Europe Support

support.europe@everspin.com

Japan

Everspin Japan Support

support.japan@everspin.com

Asia Pacific

Everspin Asia Support

support.asia@everspin.com

Filename:

EST00183_MR0A08B_Datasheet_Rev8.6032218

Everspin Technologies, Inc.

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate any integrated circuit or circuits based on the information in this document. Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals" must be validated for each customer application by customer's technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part. Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc. All other product or service names are the property of their respective owners.

Copyright © Everspin Technologies, Inc. 2018

